REMARKS/ARGUMENTS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 3, 4, 6-8, 11, 12 and 18 are presently pending in this application, Claim 18 having been added by the present amendment.

In the outstanding Office Action, the specification was objected for informality; and Claims 1-4 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sakamoto et al. (U.S. Patent 6,687,985) in view of Londa (U.S. Patent 5,963,430).

The specification has been amended to correct the noted informality.

Claim 1 has been amended to clarify the subject matter recited therein and Claim 18 has been added herein. These amendment and addition in the claims find support in the specification, claims and/or drawings as originally filed, and no new matter is believed to be added thereby. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work in a joint effort to derive mutually satisfactory claim language.

Briefly recapitulating, Claim 1 is directed to a multi-layer printed wiring board and recites: "a first substrate having an opening and having a plurality of external terminals positioned to be connected to a package substrate; a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion; and an IC component having a plurality of terminals and loaded in the opening of the first substrate such that the terminals of the IC component face an opposite side of the metallic layer portion of the second substrate, wherein the IC chip is

accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC chip."

By providing such a second substrate, heat generated by the IC component is effectively radiated to and removed through the metallic layer portion and the non-through holes connected to the metallic layer portion in the second substrate, thereby preventing heat damage caused by the IC component.

The Office Action states that "Sakamoto et al. discloses a multi-layer printed wiring board as shown in figure 1 comprising ... a second substrate (11a) laminated to the first substrate (12, 11b) having a plurality of terminals ... and having a metallic layer (electrodes 22) in the opening (15) of the first substrate (12, 11b) and a plurality of non-through holes (see figure 1) filled with conductive materials and electrically connected to the metallic layer (22), a carrier board (16) having terminals (21) formed in the opening and connected to the metallic layer (22) of the second substrate (11a)" and that "[i]t would have been obvious ... to have a teaching of Londa employed in the wiring board of Sakamoto et al. in order to form a multi-electronic/chip package."

However, it is respectfully submitted that Sakamoto et al. and Londa do not teach or suggest "a second substrate laminated to the first substrate and having a plurality of external terminals positioned to be connected to a mother board, the second substrate having a metallic layer portion in the opening of the first substrate and a plurality of non-through holes filled with conductive material and connected to the metallic layer portion ..., wherein the IC chip is accommodated in the opening such that the metallic layer portion and non-through holes of the second substrate irradiate heat generated by the IC chip" as recited in amended Claim 1.

Specifically, Sakamoto et al. simply shows a structure in which a carrier board 16 is set in a cavity 15 of a mother board 11 and electrically connected to the mother board 11, and

electrodes 22 are connected to carrier board electrodes when the carrier board 16 is set in the mother board 11. As such, Sakamoto et al. clearly fails to disclose a substrate having a metallic layer and non-through holes connected to the metallic layer which are structured in a manner that heat generated by an IC chip accommodated in an opening of another substrate is irradiated. Hence, even assuming *arguendo* that the teachings of Londa is combined with Sakamoto et al., a resulted device would not satisfy each and every element recited in Claim 1. Therefore, the structure recited in Claim 1 is believed to be distinguishable from Sakamoto et al. and Londa, and because Sakamoto et al. and Londa fail to disclose the second substrate as recited in amended Claim 1, their teachings even in combination do not render the multi-layer printed wiring board recited in Claim 1 obvious.

For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 3, 4, 6-8, 11, 12 and 18 depend directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 3, 4, 6-8, 11, 12 and 18 are believed to be allowable as well.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

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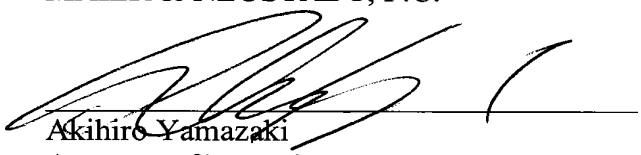

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